



# FPGA设计思维

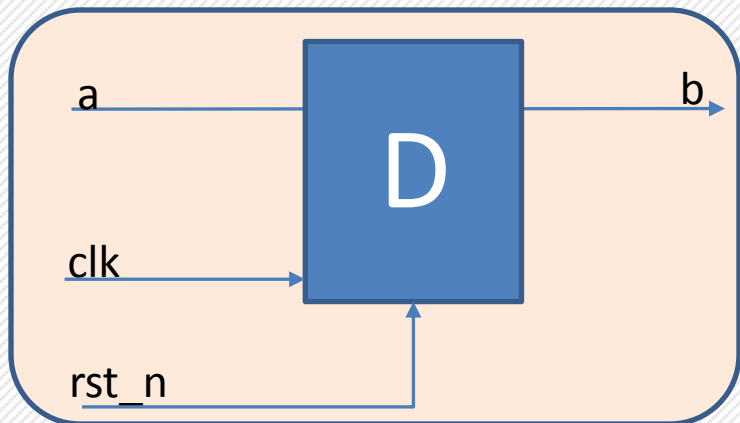
主讲人：潘老师



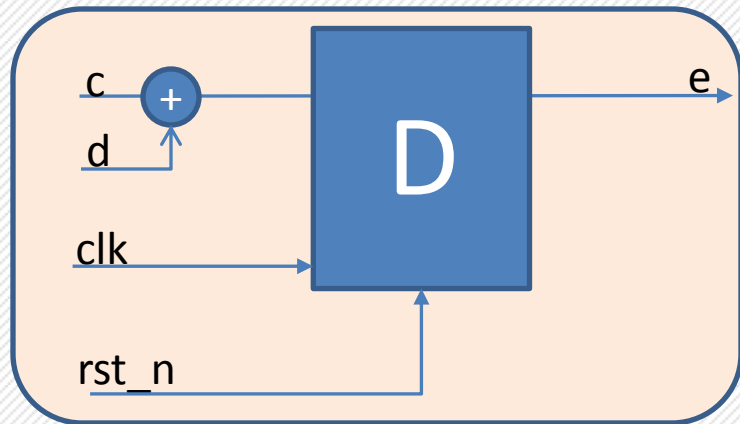
**SiMPLE** DESIGN



# 硬件思维设计



```
always @(posedge clk or negedge rst_n)begin
    if(rst_n==1'b0)begin
        b <= 0;
    end
    else begin
        b <= a;
    end
end
```



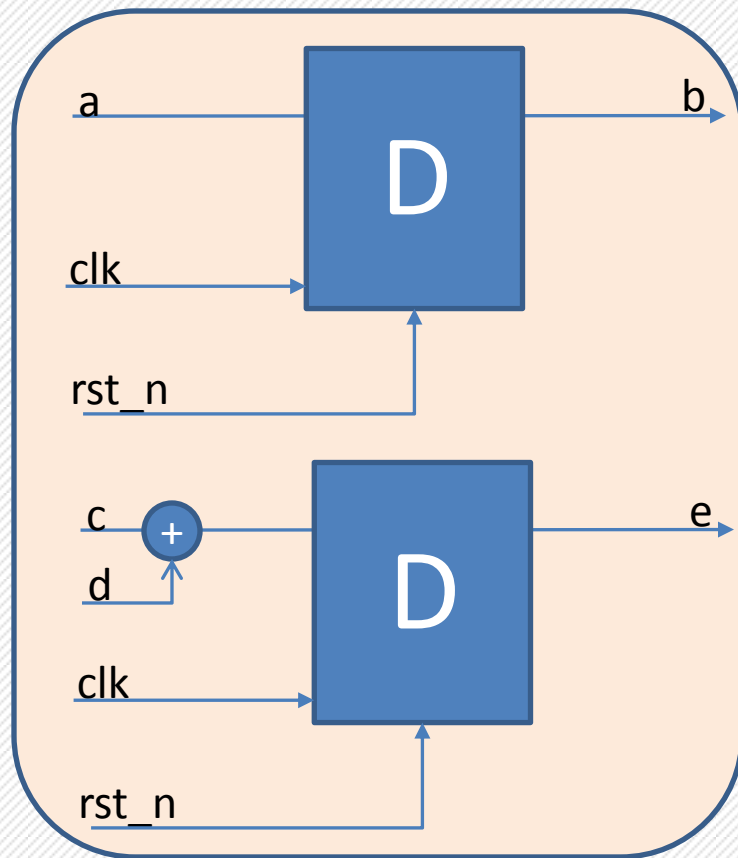
```
always @(posedge clk or negedge rst_n)begin
    if(rst_n==1'b0)begin
        e <= 0;
    end
    else begin
        e <= c + d;
    end
end
```

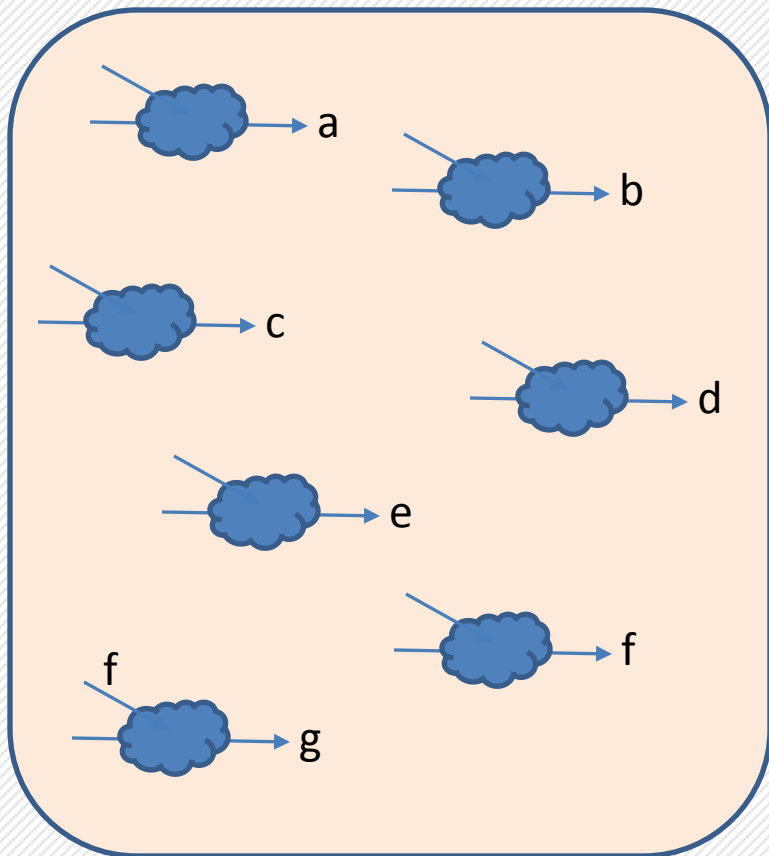


# 硬件思维设计

```
always @(posedge clk or negedge rst_n) begin
    if(rst_n==1'b0) begin
        b <= 0;
    end
    else begin
        b <= a;
    end
end

always @(posedge clk or negedge rst_n) begin
    if(rst_n==1'b0) begin
        e <= 0;
    end
    else begin
        e <= c + d;
    end
end
```



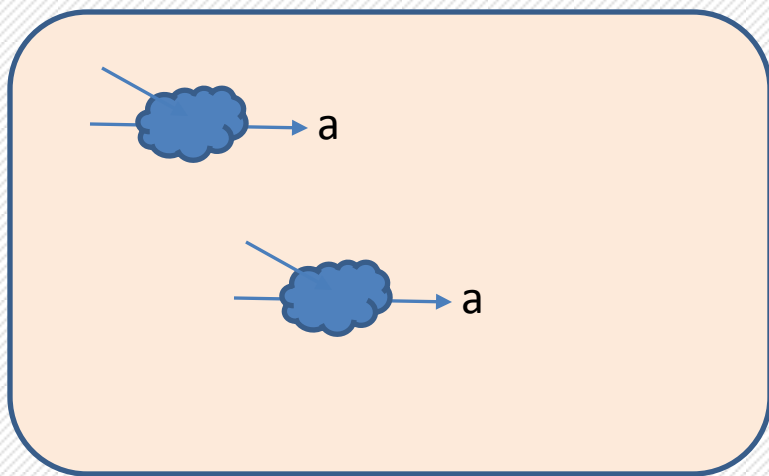


```

always @(posedge clk or negedge rst_n)begin
    if(rst_n==1'b0)begin
        a <= 0;
    end
    else begin
        a <= xxxx;
    end
end

always @(posedge clk or negedge rst_n)begin
    if(rst_n==1'b0)begin
        b <= 0;
    end
    else begin
        b <= yyyy;
    end
end

省略.....|
always @(posedge clk or negedge rst_n)begin
    if(rst_n==1'b0)begin
        g <= 0;
    end
    else begin
        g <= zzzzzzz;
    end
end
    
```



一个信号不可能在多个always设计

```
always @(posedge clk or negedge rst_n) begin
    if(rst_n==1'b0) begin
        a <= 0;
    end
    else if(b==1) begin
        a <= 1;
    end
end

always @(posedge clk or negedge rst_n) begin
    if(rst_n==1'b0) begin
        a <= 0;
    end
    else if(c==1) begin
        a <= 0;
    end
end
```



## 思维对比

```
always @(posedge clk or negedge rst_n) begin
    if(rst_n==1'b0) begin
        cnt <= 0;
    end
    else if(add_cnt) begin
        cnt <= cnt + 1;
        if(cnt==10)
            cnt <= 0;
    end
end
```

```
always @(posedge clk or negedge rst_n) begin
    if(rst_n==1'b0) begin
        cnt <= 0;
    end
    else if(add_cnt) begin
        if(cnt==10)
            cnt <= 0;
        else
            cnt <= cnt +1;
    end
end
```



## 总结要点

1. 一个信号就是一个元器件。
2. 一个always/模块就是一个元器件。
3. 设计的思路：逐个定义好每个信号/元器件的功能，然后连接起来。
4. 怎么想每个信号的功能，从而实现最终目标？画波形！请看接下来视频。

# THANKS

