明德扬
科技.教育

点拨·FPGA之
Verilog快速掌握之模块设计

点透学习误区　　拨出设计精髓

主　讲：潘文明

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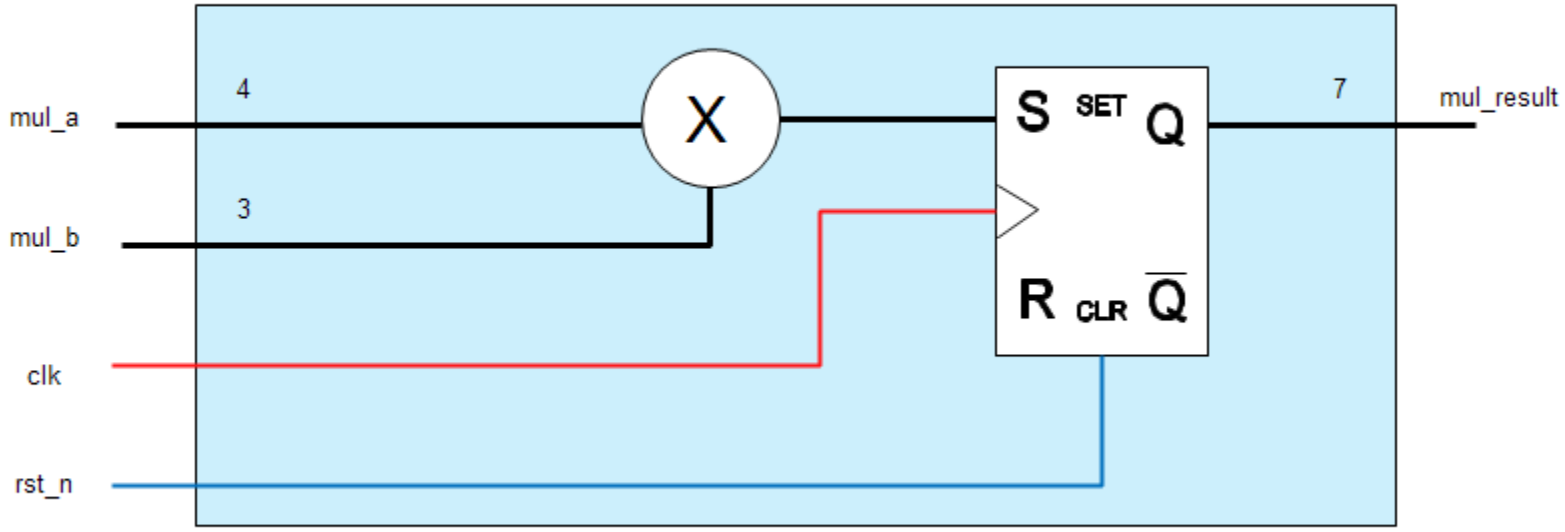
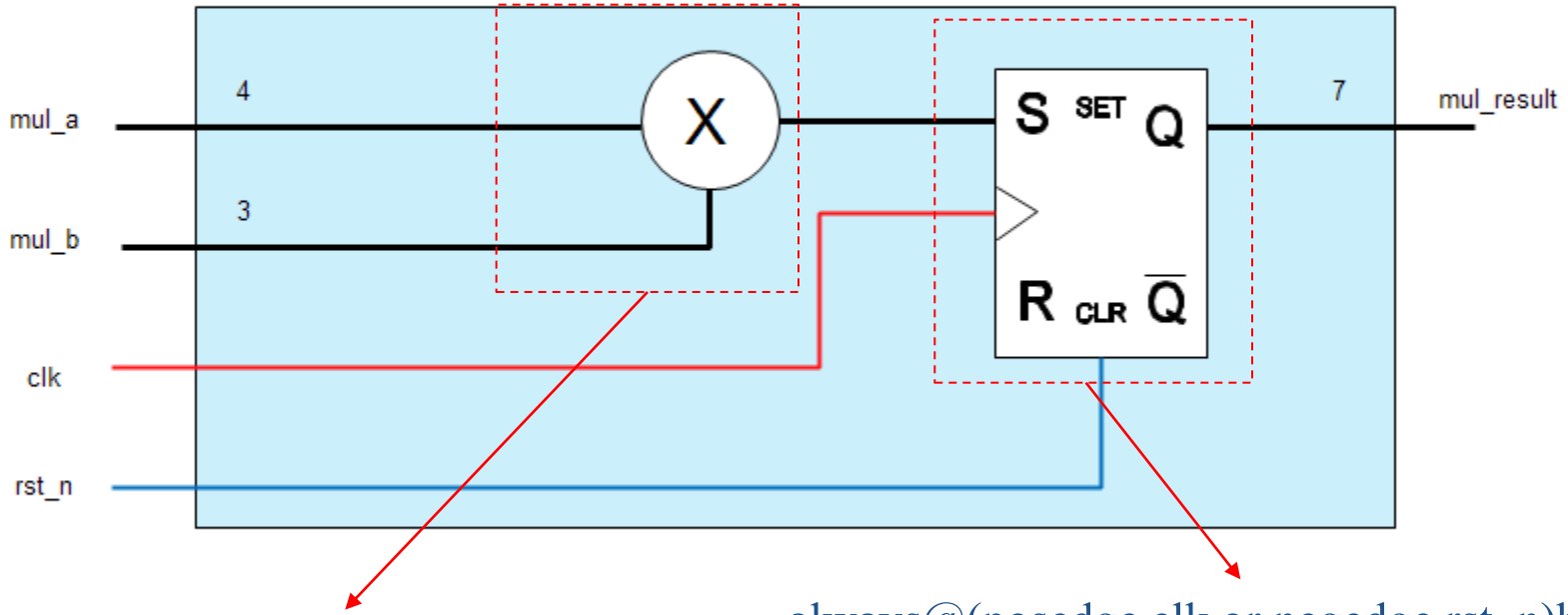
Verilog代码详细讲解



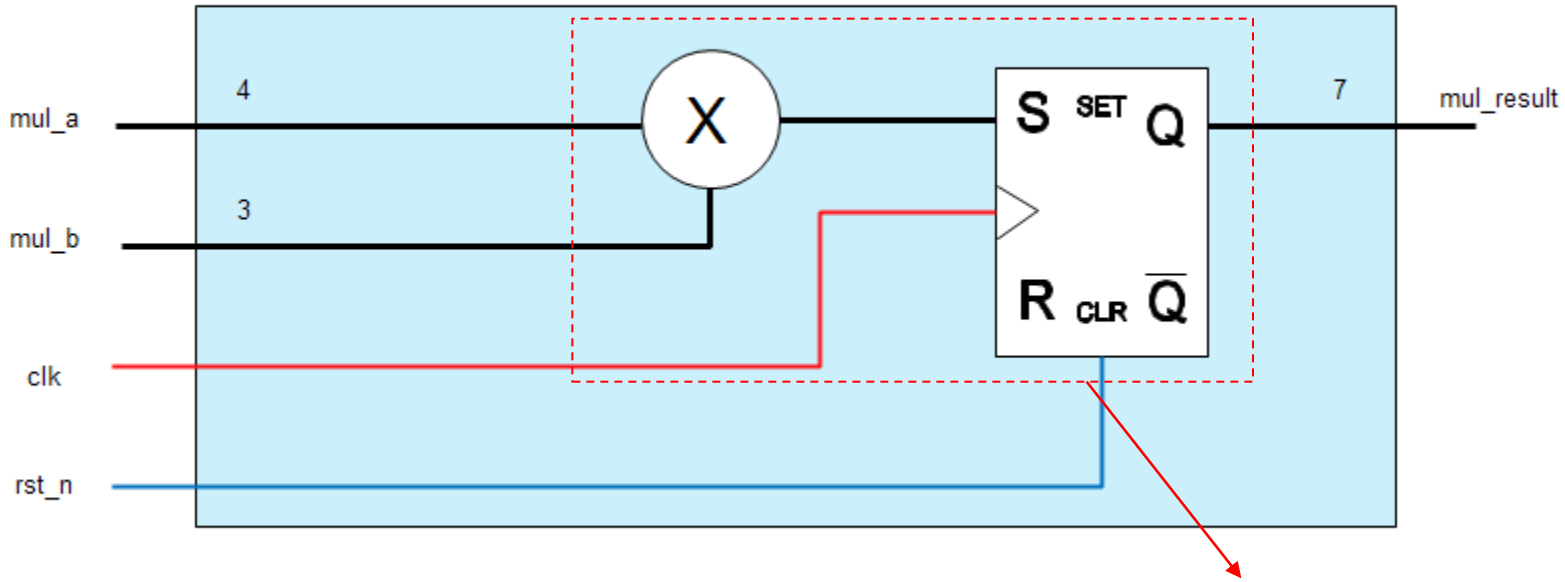
Verilog代码详细讲解




```
always@(*)begin
      mul_result_tmp = mul_a * mul_b;
   end
```

```
always@(posedge clk or negedge rst_n)begin
      if(rst_n==1'b0)begin
         mul_result <= 0;
      end
      else begin
         mul_result <= mul_result_tmp;
      end
   end
```

Verilog代码详细讲解




```
always@(posedge clk or negedge rst_n)begin
    if(rst_n==1'b0)begin
        mul_result <= 0;
    end
    else begin
        mul_result <= mul_a * mul_b;
    end
end
```

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Thank You !