VIVADO时序原理

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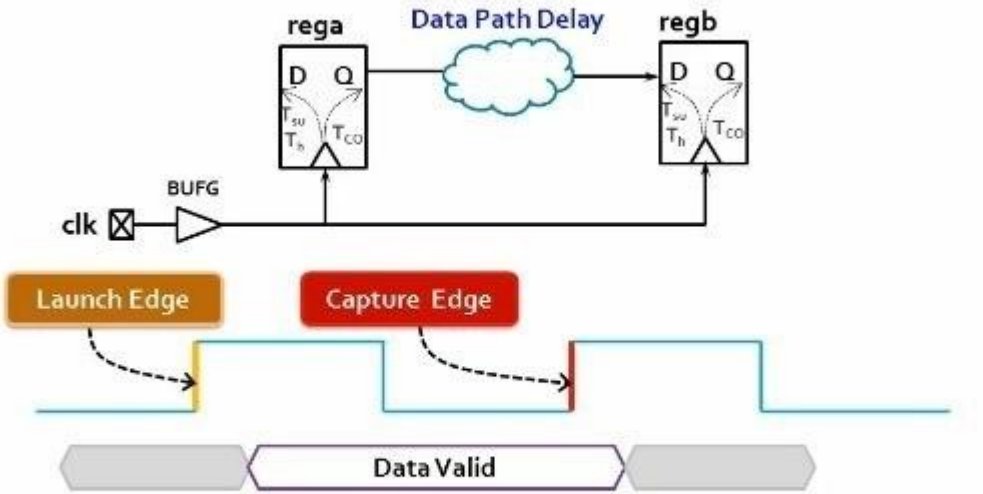
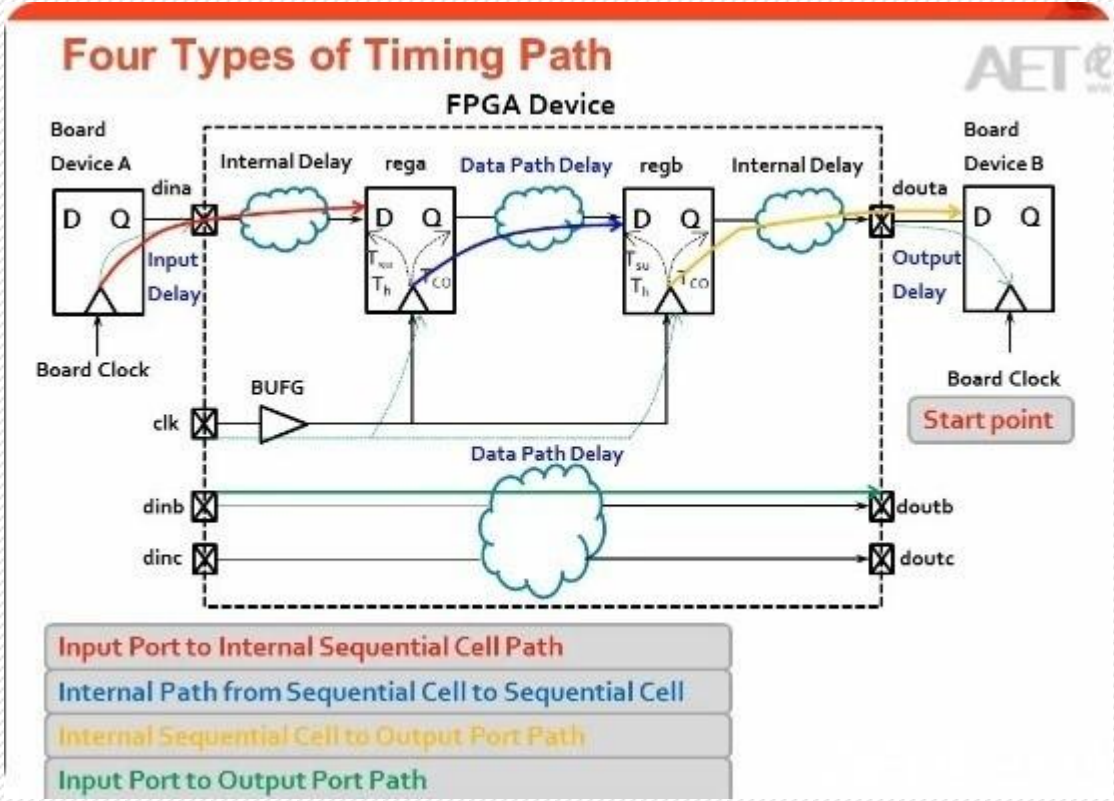
MDY

SiMPLE DESIGN

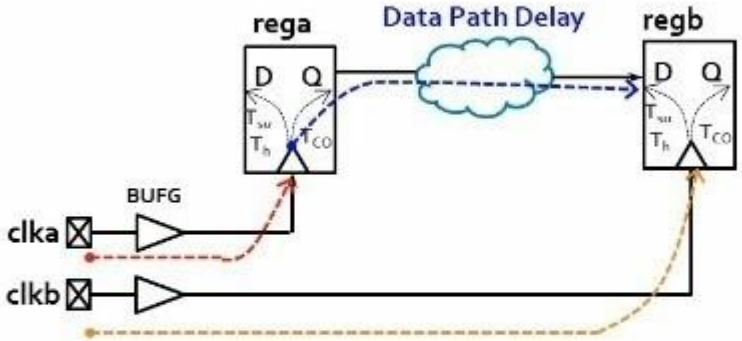
Launch vs. Capture Edges



Launch Edge : the edge which "launches" the data from source register
Capture Edge : the edge which "captures" the data at destination register
(with respect to the launch edge, selected by timing analyzer; typically 1 cycle)


Four Types of Timing Path
FPGA Device
Board
Device A
dina
Internal Delay
rega
Data Path Delay
regb
Internal Delay
douta
Board
Device B
D Q
Input
Delay
Output
Delay
Board Clock
BUFG
clk
Start point
Data Path Delay
dinb
dinc
doutb
doutc
Input Port to Internal Sequential Cell Path
Internal Path from Sequential Cell to Sequential Cell
Internal Sequential Cell to Output Port Path
Input Port to Output Port Path

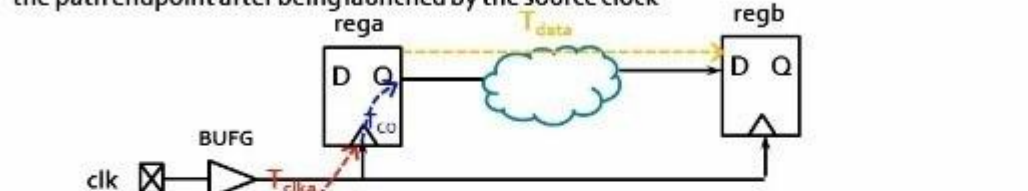
Timing Path Sections



Path	Start Point	End Point
Source Clock Path	Clk input port	Clk pin of launch reg
Data Path	Clk pin of launch reg	Data input pin of capture reg
Destination Clock Path	Clk input port	Clk pin of ca[illegible] re[illegible] eg

Data Arrival Time

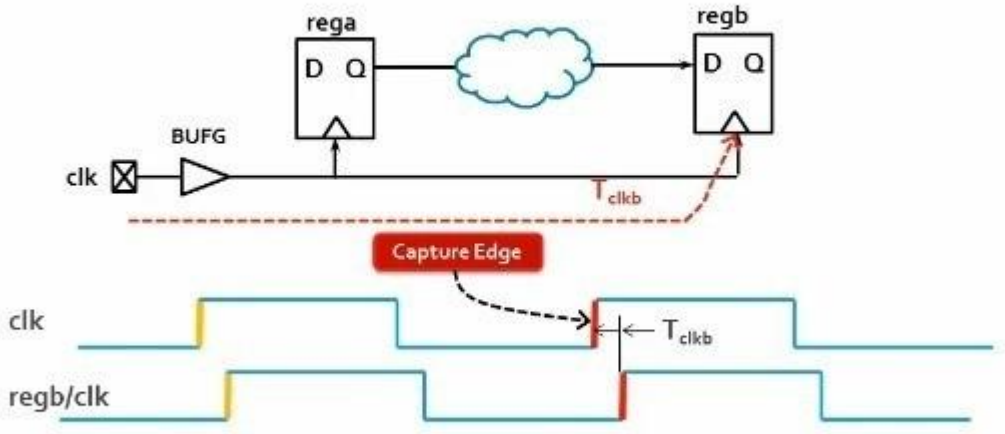
The data arrival time for setup analysis is the time it takes for the data to be stable at the path endpoint after being launched by the source clock



Data Arrival Time = Launch Edge + T_{clka} + T_{co} + T_{data}

Clock Arrival Time

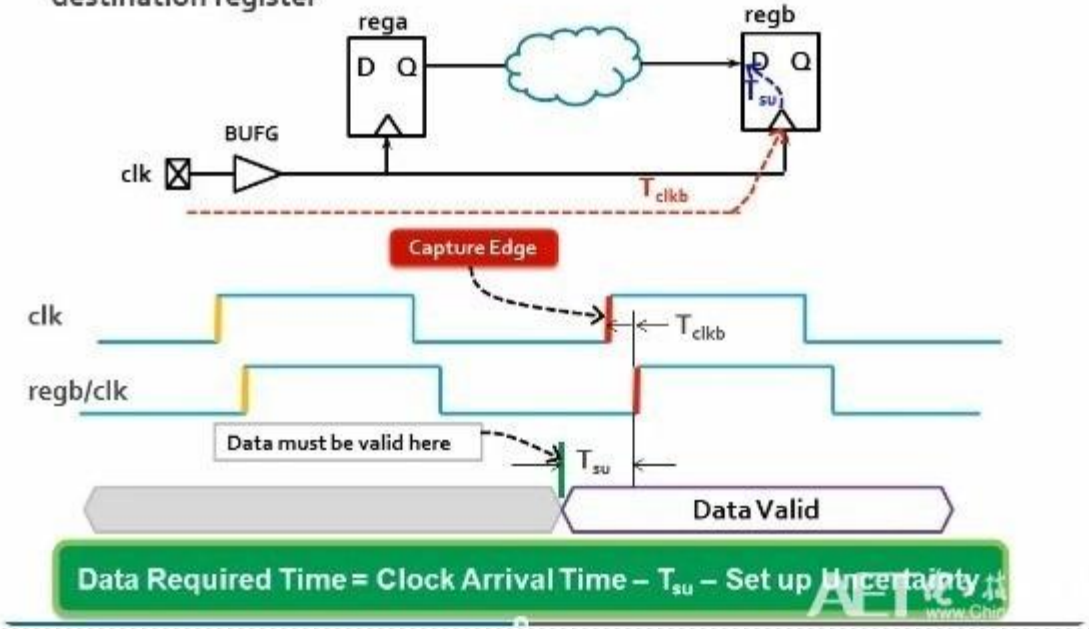
The time for clock to arrive destination register's clock input pin

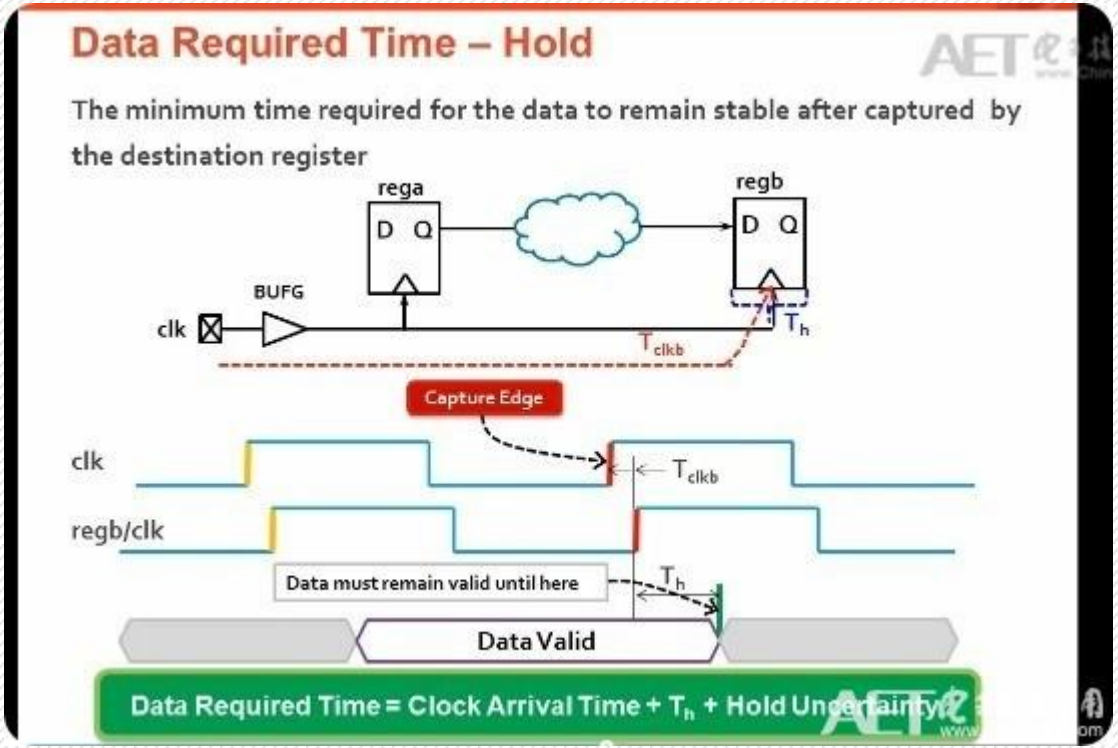


Clock Arrival Time = Capture Edge + T_{clkb}

Data Required Time – Set up

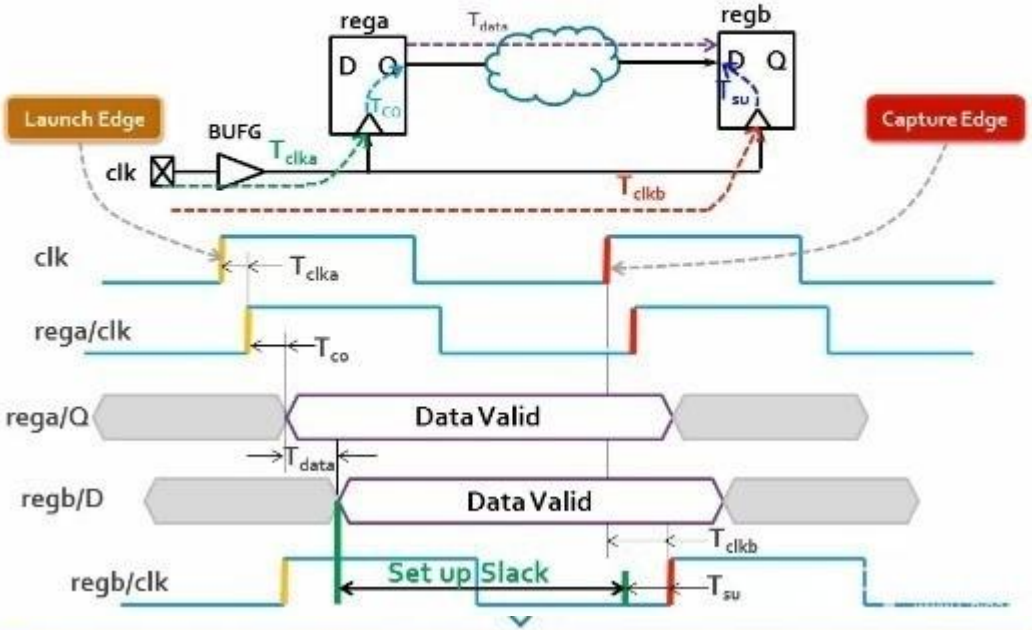
The minimum time required for the data to get captured by the destination register




Data Required Time – Hold
The minimum time required for the data to remain stable after captured by the destination register
rega
regb
D Q
D Q
BUFG
clk
T_{clkb}
T_h
Capture Edge
clk
T_{clkb}
regb/clk
Data must remain valid until here
T_h
Data Valid
Data Required Time = Clock Arrival Time + T_h + Hold Uncertainty

Setup Slack

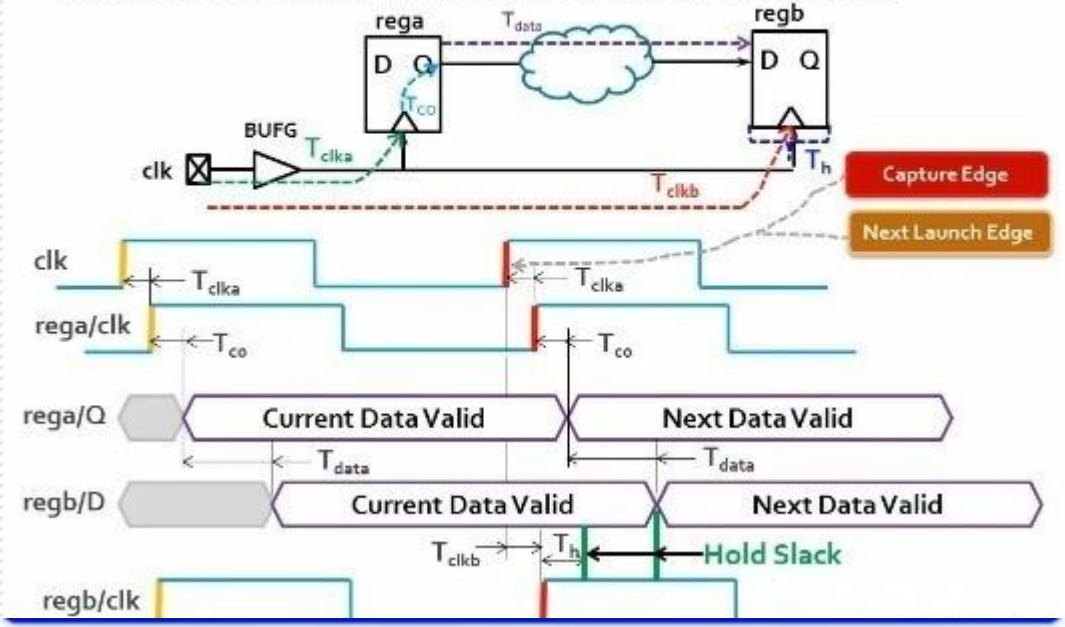
The margin by which the setup timing requirement is met. It ensures launched data arrives in time to meet the capturing requirement



Setup Slack = Data Required Time (Setup) – Data Arrival Time (Setup)

Hold Slack

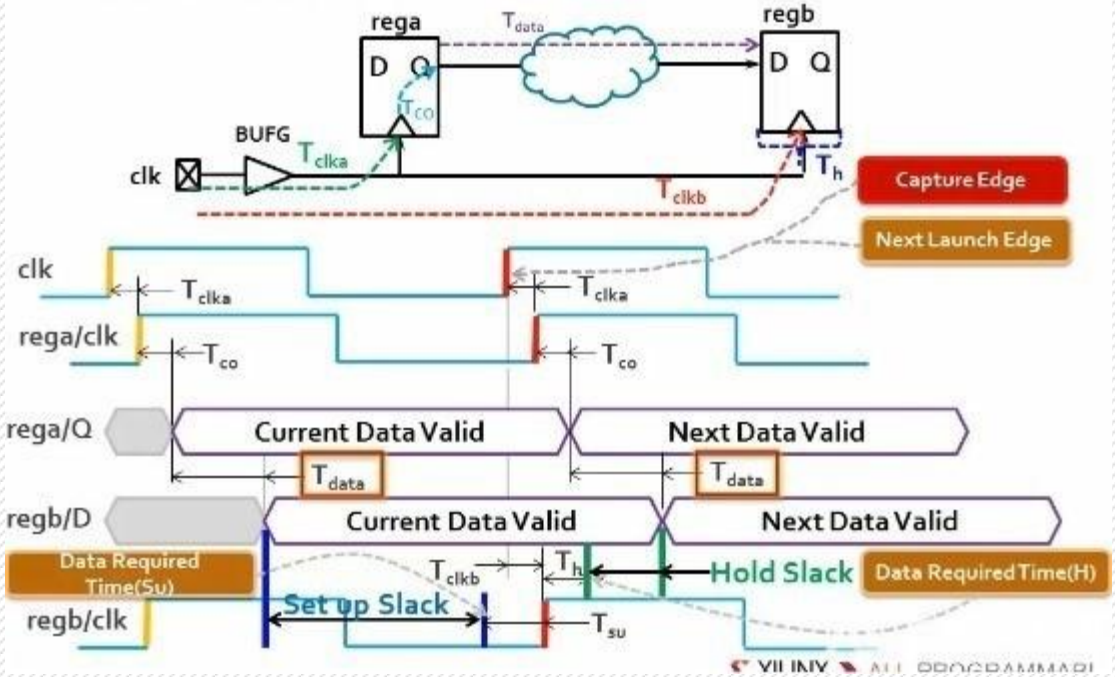
The margin by which the hold timing requirement is met. It ensures capture data is not corrupted by data from another launch edge. It also prevents "double-clocking"



Hold Slack = Data Arrival Time (Hold) – Data Required Time (Hold)

Setup & Hold Slack

The margin by which the hold timing requirement is met. It ensures capture data is not corrupted by data from another launch edge. It also prevents "double-clocking"



Slack Equations

Data Required Time (Setup) = Clock Arrival Time – T_{su} – Set up Uncertainty

Data Required Time (Hold) = Clock Arrival Time + Th + Hold Uncertainty

Setup Slack = Data Required Time (Setup) – Data Arrival Time (Setup)

Hold Slack = Data Arrival Time (Hold) – Data Required Time (Hold)

Positive slack: Timing requirement met

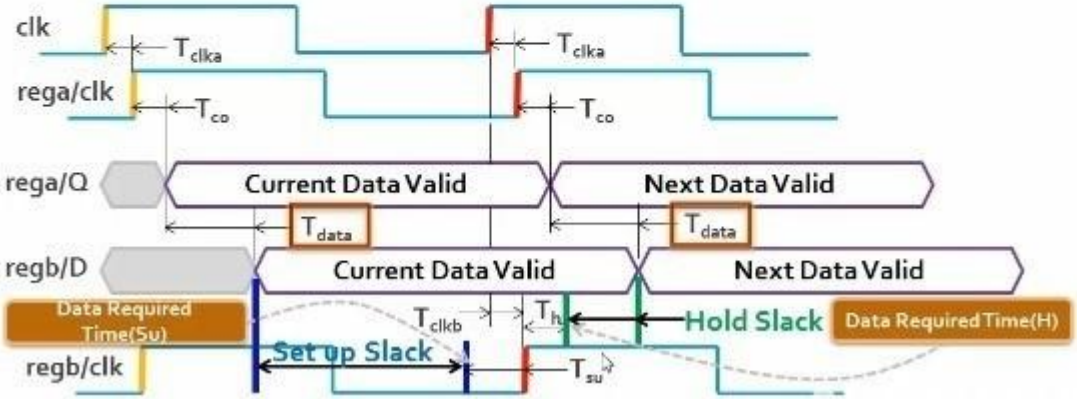
Negative slack: Timing requirement not met

Equations work for all timing path: Interal, I/O & asynchronous control

Why Is Slack Negative?

Setup Slack = Data Required Time (Setup) – Data Arrival Time (Setup)

Hold Slack = Data Arrival Time (Hold) – Data Required Time (Hold)



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System Frequency

$$T_{data} = T_{\log ic} + T_{net}$$

$$T_s \geq T_{CO} + T_{data} + T_{su}$$

Summary

- Launch edge time is used as reference point during timing analysis
- Normally, capture edge time = launch edge time + 1 clock cycle
- T_{su} and T_h are dependent on the device which cannot be changed

THANKS